BURIED CHANNEL DEVICES AND A PROCESS FOR THEIR FABRICATION SIMULTANEOUSLY WITH SURFACE CHANNEL DEVICES TO PRODUCE TRANSISTORS AND CAPACITORS WITH MULTIPLE ELECTRICAL GATE OXIDES

ABSTRACT OF THE DISCLOSURE

A method for fabricating buried channel NMOS devices and the devices themselves are disclosed. These buried channel NMOS devices are fabricated with a p-type substrate, an n-type implant in the top portion (approximately 400 to 1000 Å deep) of the substrate, and an insulating gate dielectric above the n-type implant. An n-type or p-type doped polysilicon gate electrode is formed on top of the insulating gate dielectric. The n-type implant region is doped in such a way that it is depleted of charge carriers when the device's gate electrode is at the same potential as the well (zero bias). When the gate electrode is biased $+V_e$ with respect to the device's well substrate a conducting channel of mobile electrons is formed in a portion of the buried layer. This type of biasing is known as inversion bias since the charge carriers are of the opposite type than the p-well. Under inversion bias, the buried channel silicon region is partially depleted of charge carriers, which effectively adds to the thickness of the gate dielectric layer. A capacitor or transistor fabricated according to this buried channel teaching behaves in a manner electrically equivalent to a capacitor or transistor fabricated with a thicker dielectric. PMOS transistors and capacitors can be constructed according to the present invention in a manner similar to that described for NMOS transistors and capacitors by substituting n-type doping for p-type and visa versa. This leads to the fabrication of CMOS devices with multiple effective dielectric thicknesses on the same substrate.